

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

IN RE APPLICATION OF: Shinsuke SAKAMOTO, et al.

GAU:

SERIAL NO: New Divisional Application

EXAMINER:

FILED: Herewith

FOR: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND STANDARD CELL PLACEMENT  
DESIGN METHOD

**REQUEST FOR PRIORITY**

COMMISSIONER FOR PATENTS  
ALEXANDRIA, VIRGINIA 22313

SIR:

☒ Full benefit of the filing date of U.S. Application Serial Number 10/282,144, filed October 29, 2002, is claimed pursuant to the provisions of 35 U.S.C. §120.

☐ Full benefit of the filing date(s) of U.S. Provisional Application(s) is claimed pursuant to the provisions of 35 U.S.C. §119(e): Application No. Date Filed

☒ Applicants claim any right to priority from any earlier filed applications to which they may be entitled pursuant to the provisions of 35 U.S.C. §119, as noted below.

In the matter of the above-identified application for patent, notice is hereby given that the applicants claim as priority:

<u>COUNTRY</u>	<u>APPLICATION NUMBER</u>	<u>MONTH/DAY/YEAR</u>
Japan	2001-331294	October 29, 2001

Certified copies of the corresponding Convention Application(s)

☐ are submitted herewith

☐ will be submitted prior to payment of the Final Fee

☒ were filed in prior application Serial No. 10/282,144 filed October 29, 2002

☐ were submitted to the International Bureau in PCT Application Number  
Receipt of the certified copies by the International Bureau in a timely manner under PCT Rule 17.1(a) has been acknowledged as evidenced by the attached PCT/IB/304.

☐ (A) Application Serial No.(s) were filed in prior application Serial No. filed ; and

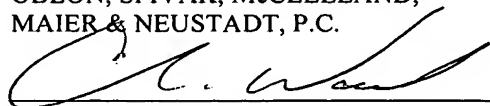
☐ (B) Application Serial No.(s)

☐ are submitted herewith

☐ will be submitted prior to payment of the Final Fee

Respectfully Submitted,

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